FIG.1

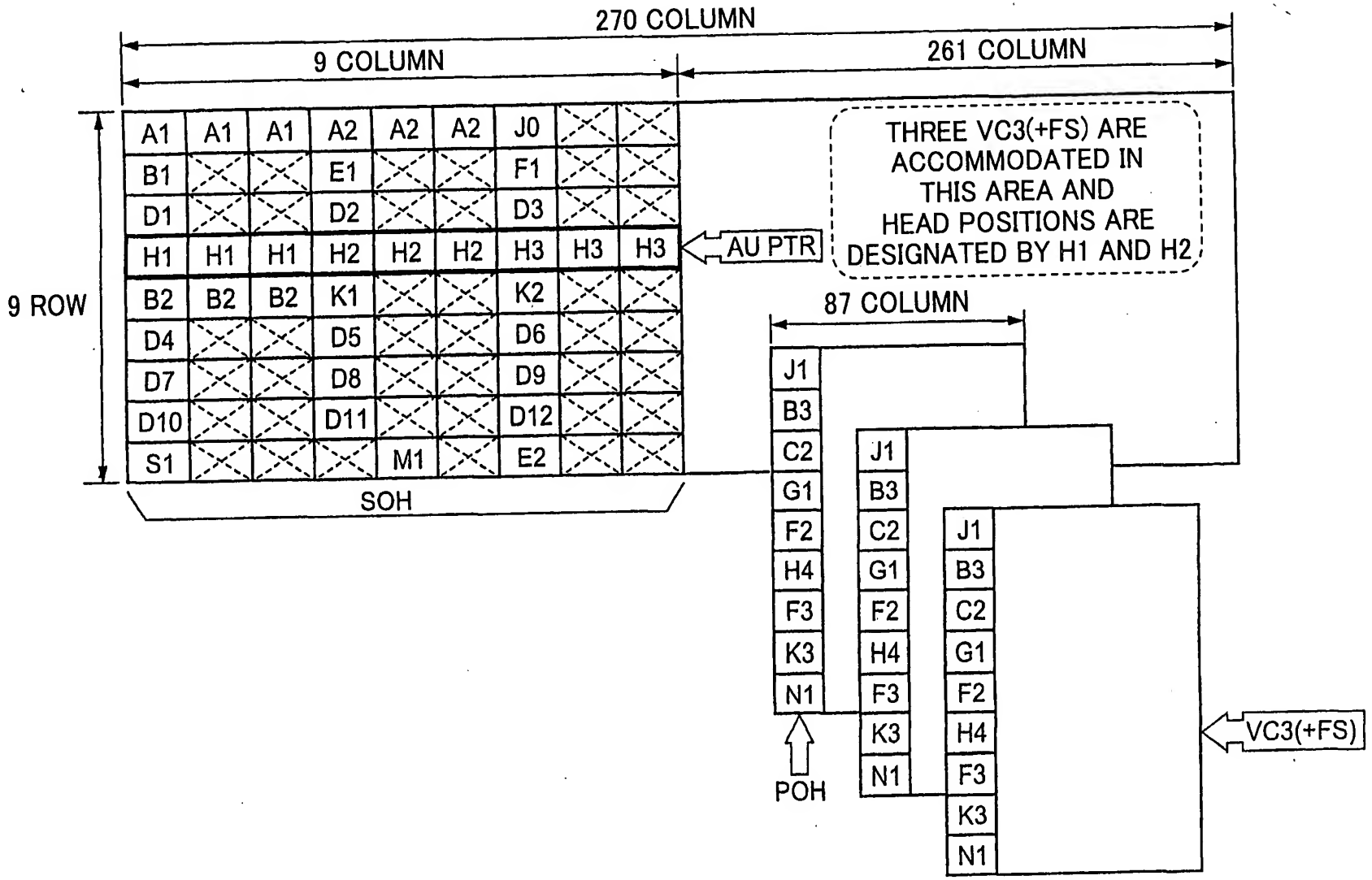

270 COLUMN
9 COLUMN
261 COLUMN
9 ROW
A1 A1 A1 A2 A2 A2 J0
B1 E1 F1
D1 D2 D3
H1 H1 H1 H2 H2 H2 H3 H3 H3
B2 B2 B2 K1 K2
D4 D5 D6
D7 D8 D9
D10 D11 D12
S1 M1 E2
SOH
AU PTR
THREE VC3(+FS) ARE ACCOMMODATED IN THIS AREA AND HEAD POSITIONS ARE DESIGNATED BY H1 AND H2
87 COLUMN
J1 B3 C2 G1 F2 H4 F3 K3 N1
POH
VC3(+FS)

FIG.2

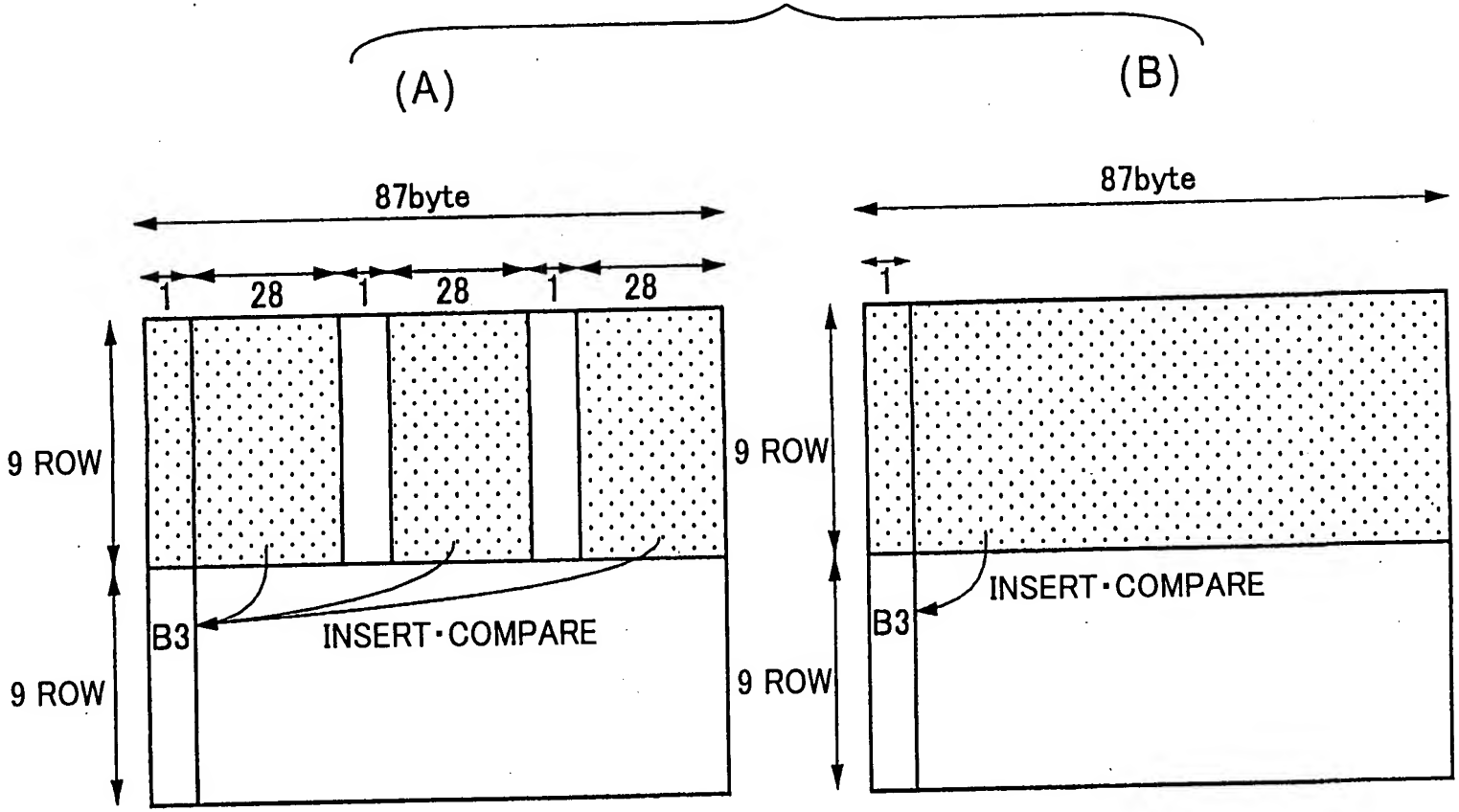

(A)
(B)
87byte
87byte
1
28
1
28
1
28
1
9 ROW
9 ROW
9 ROW
9 ROW
B3
B3
INSERT·COMPARE
INSERT·COMPARE

FIG.3

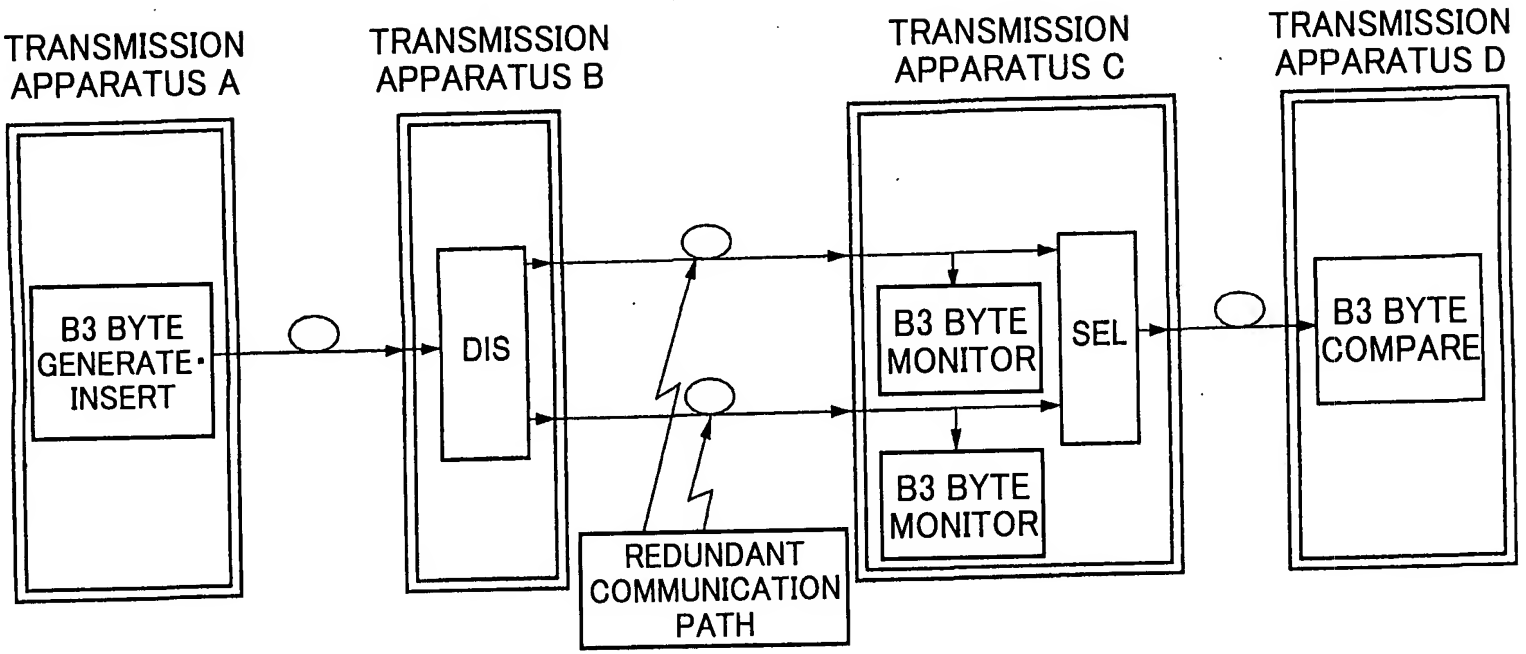

TRANSMISSION APPARATUS A
B3 BYTE GENERATE· INSERT
TRANSMISSION APPARATUS B
DIS
REDUNDANT COMMUNICATION PATH
TRANSMISSION APPARATUS C
B3 BYTE MONITOR
B3 BYTE MONITOR
SEL
TRANSMISSION APPARATUS D
B3 BYTE COMPARE

FIG.4

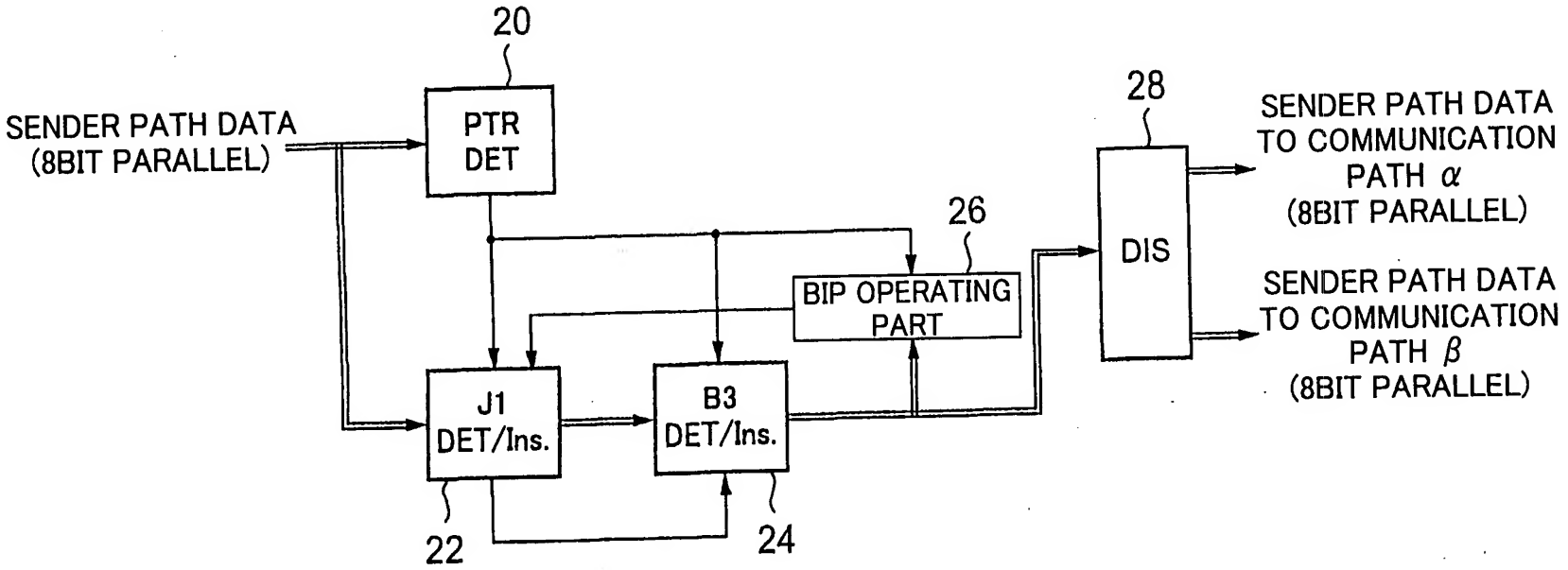

20
SENDER PATH DATA
(8BIT PARALLEL)
PTR
DET
28
SENDER PATH DATA
TO COMMUNICATION
PATH α
(8BIT PARALLEL)
26
BIP OPERATING
PART
DIS
SENDER PATH DATA
TO COMMUNICATION
PATH β
(8BIT PARALLEL)
J1
DET/Ins.
B3
DET/Ins.
22
24

FIG.5

(A) SENDER PATH DATA (J1DET/Ins. INPUT)

(B) J1 BYTE PHASE INFORMATION (FROM PTR DET)

(C) RETAINED J1 BYTE DATA

(D) DIFFERENCE BETWEEN RETAINED J1 BYTE DATA AND INSERTED OPERATION RESULT

(E) B3 BYTE PHASE INFORMATION

(F) RETAINED B3 BYTE DATA

(G) INSERTED B3 BYTE DATA

(H) SENDER PATH DATA TO COMMUNICATION PATH

(I) BIP OPERATION RESULT (BIP OPERATING PART OUTPUT)

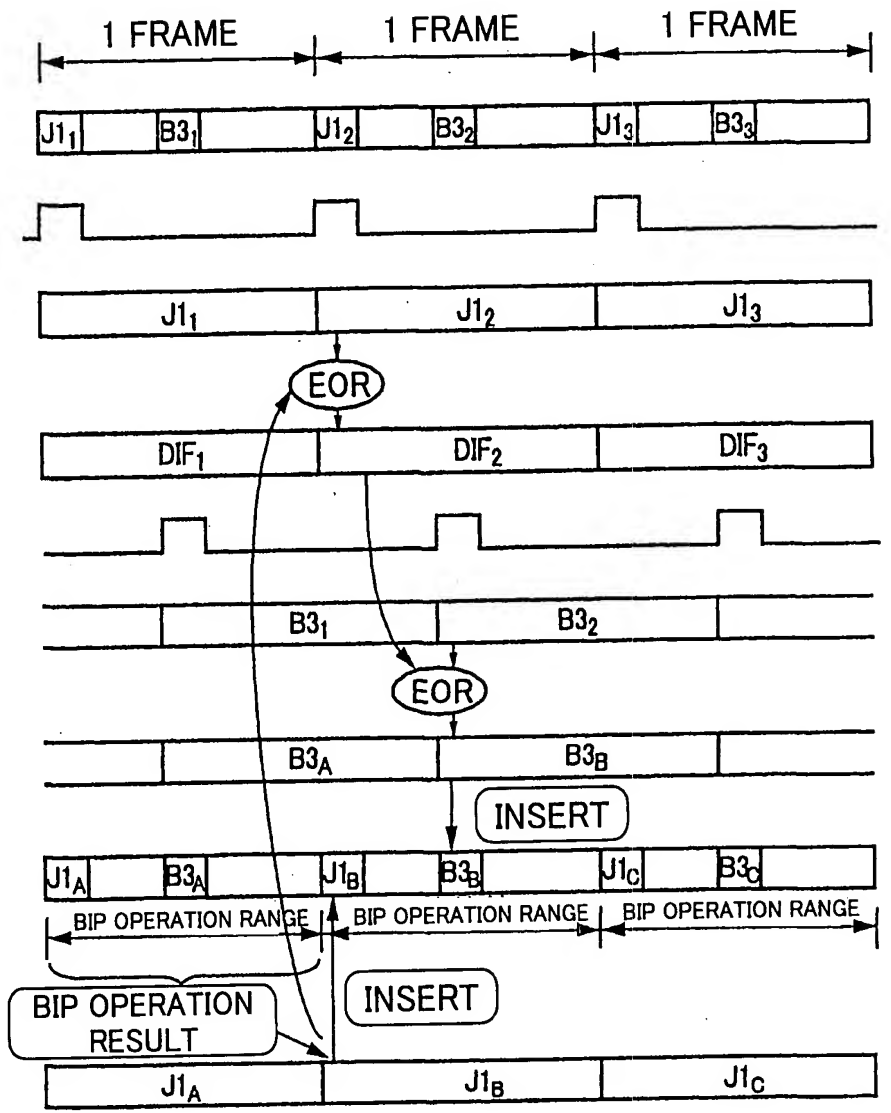


FIG.6

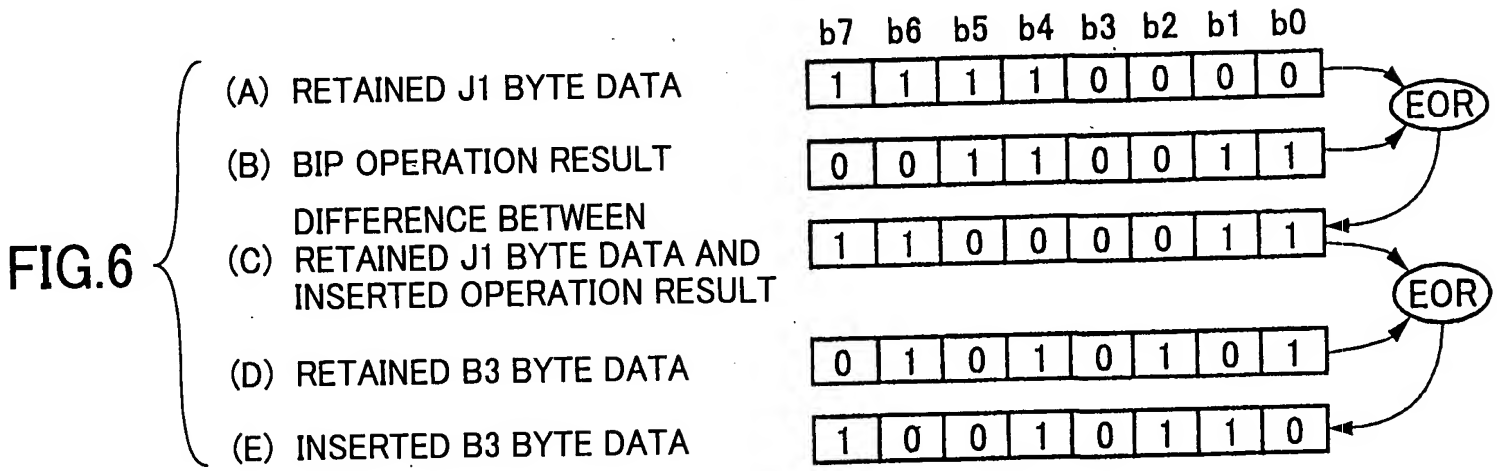

b7 b6 b5 b4 b3 b2 b1 b0
(A) RETAINED J1 BYTE DATA
1 1 1 1 0 0 0 0
(B) BIP OPERATION RESULT
0 0 1 1 0 0 1 1
EOR
(C) DIFFERENCE BETWEEN RETAINED J1 BYTE DATA AND INSERTED OPERATION RESULT
1 1 0 0 0 0 1 1
(D) RETAINED B3 BYTE DATA
0 1 0 1 0 1 0 1
EOR
(E) INSERTED B3 BYTE DATA
1 0 0 1 0 1 1 0

FIG.7

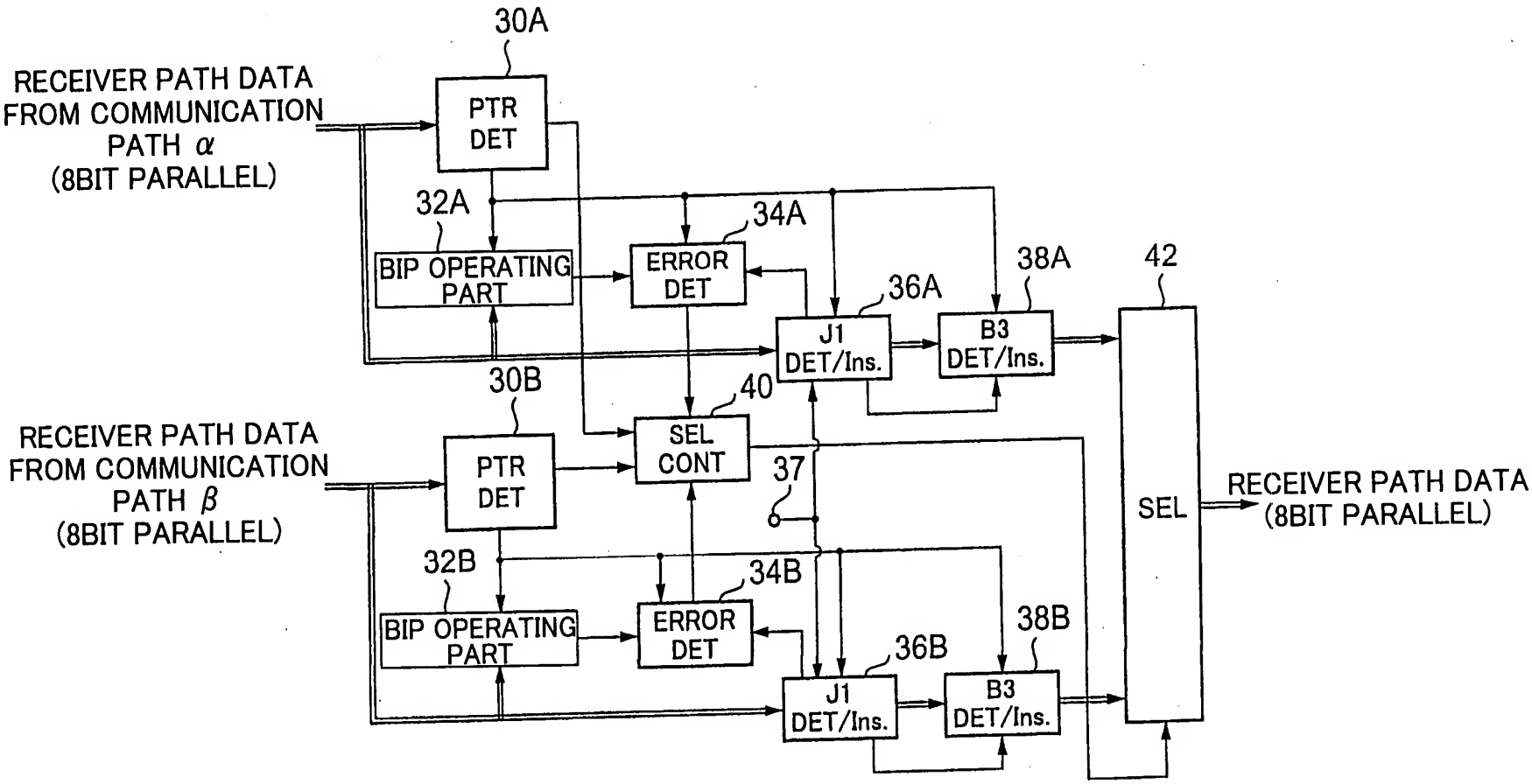

30A
RECEIVER PATH DATA FROM COMMUNICATION PATH α (8BIT PARALLEL)
PTR DET
32A
BIP OPERATING PART
34A
ERROR DET
36A
J1 DET/Ins.
38A
B3 DET/Ins.
42
30B
RECEIVER PATH DATA FROM COMMUNICATION PATH β (8BIT PARALLEL)
PTR DET
40
SEL CONT
37
32B
BIP OPERATING PART
34B
ERROR DET
36B
J1 DET/Ins.
38B
B3 DET/Ins.
SEL
RECEIVER PATH DATA (8BIT PARALLEL)

FIG.8

(A) RECEIVER PATH DATA FROM COMMUNICATION PATH (J1DET/Ins. BIP OPERATION INPUT)

(B) BIP OPERATION RESULT (BIP OPERATING PART OUTPUT)

(C) COMPARISON RESULT BETWEEN BIP OPERATION RESULT AND J1 BYTE

(D) J1 BYTE PHASE INFORMATION (FROM PTR DET)

(E) INSERTED J1 BYTE DATA (FIXED VALUE IN THIS EXAMPLE)

(F) RETAINED J1 BYTE DATA

(G) DIFFERENCE BETWEEN RETAINED J1 BYTE DATA AND INSERTED J1 BYTE DATA

(H) B3 BYTE PHASE INFORMATION (FROM PTR DET)

(I) RETAINED B3 BYTE DATA

(J) INSERTED B3 BYTE DATA

(K) RECEIVER PATH DATA TO SEL

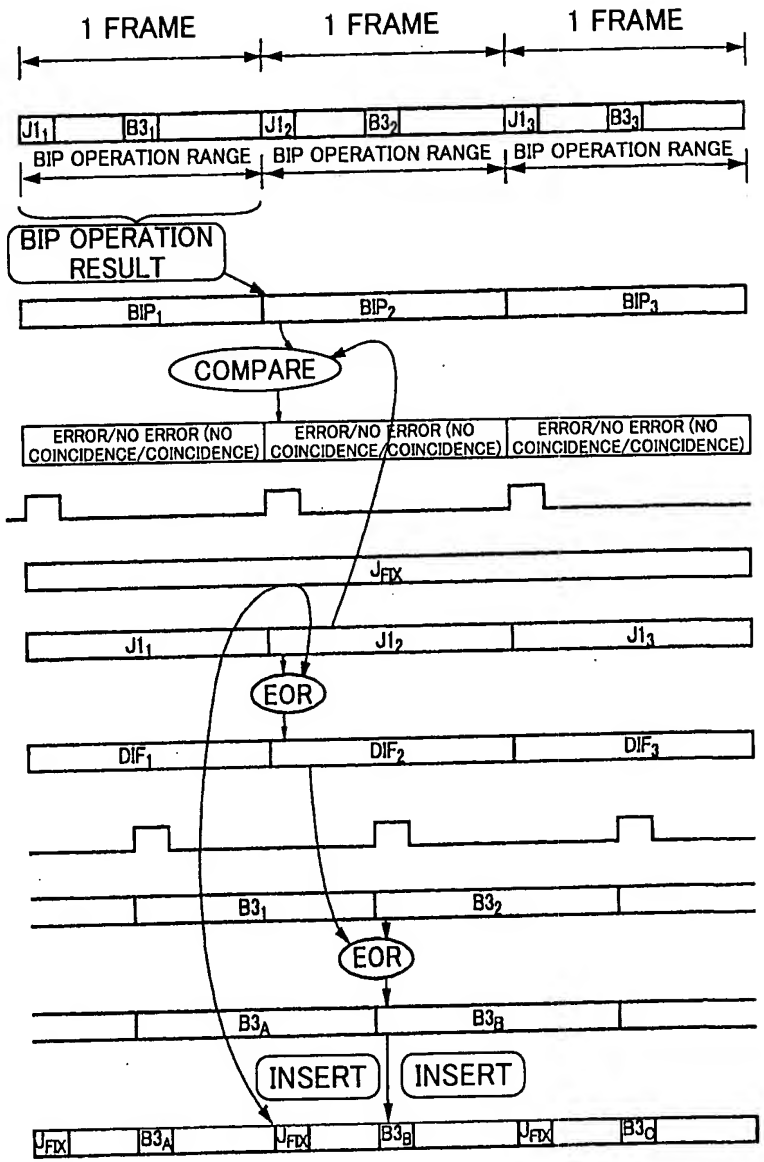


FIG.9

			CONDITION OF COMMUNICATION PATH α		
			PATH ALARM	NO PATH ALARM	
				ERROR	NO ERROR
CONDITION OF COMMUNICATION PATH β	PATH ALARM		H	α	α
	NO PATH ALARM	ERROR	β	H	α
		NO ERROR	β	β	H

FIG.10

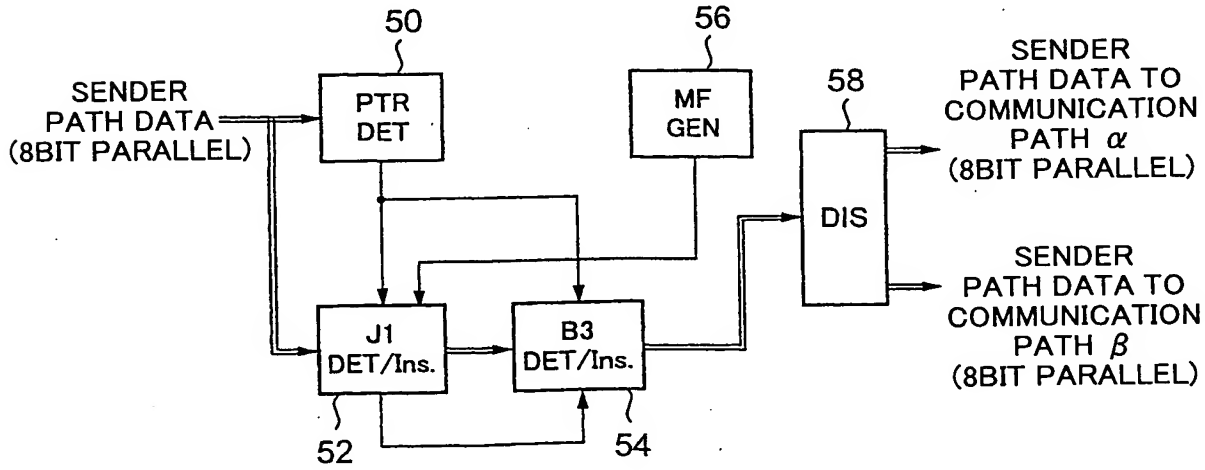


FIG.11

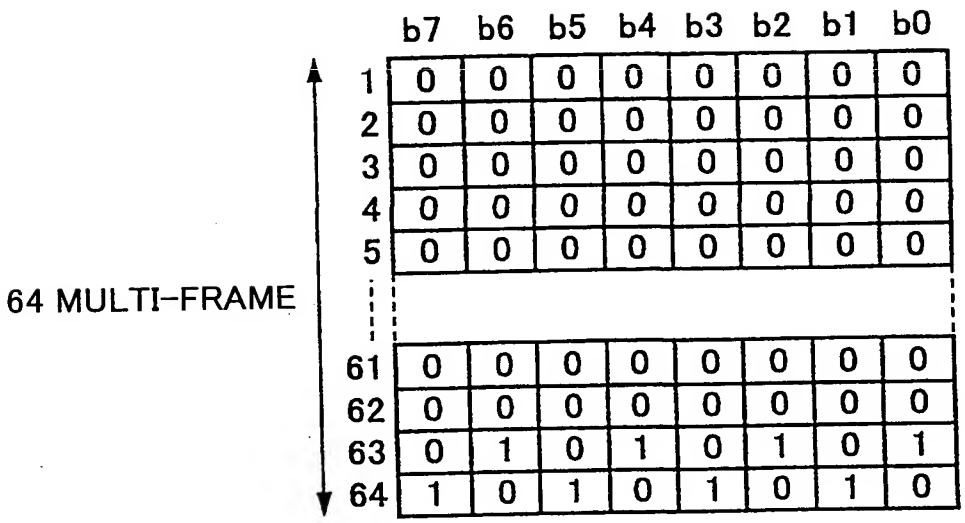

b7 b6 b5 b4 b3 b2 b1 b0
1 0 0 0 0 0 0 0 0
2 0 0 0 0 0 0 0 0
3 0 0 0 0 0 0 0 0
4 0 0 0 0 0 0 0 0
5 0 0 0 0 0 0 0 0
64 MULTI-FRAME
61 0 0 0 0 0 0 0 0
62 0 0 0 0 0 0 0 0
63 0 1 0 1 0 1 0 1
64 1 0 1 0 1 0 1 0

FIG.12

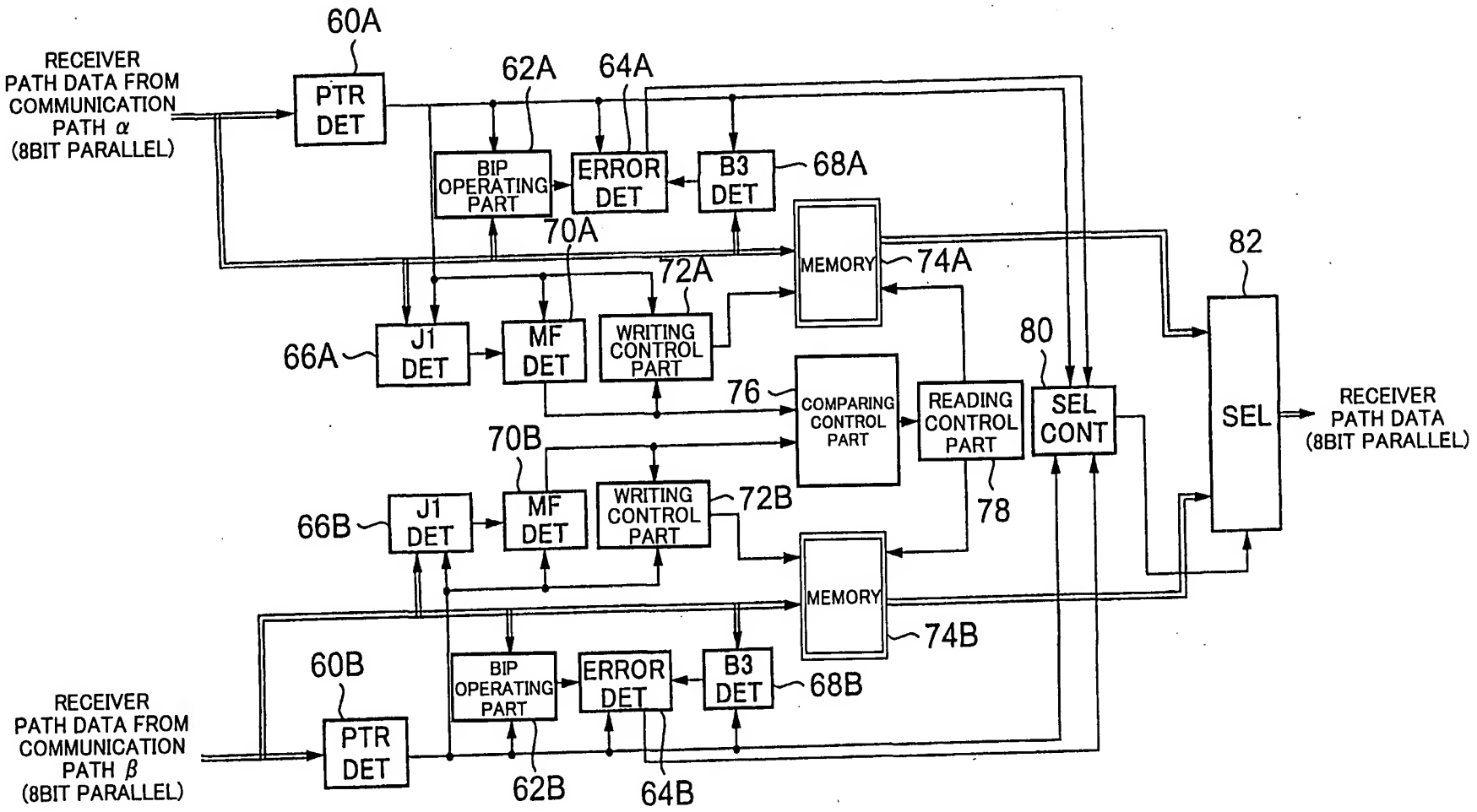

RECEIVER PATH DATA FROM COMMUNICATION PATH α (8BIT PARALLEL)
60A
PTR DET
62A
64A
BIP OPERATING PART
ERROR DET
B3 DET
68A
70A
72A
MEMORY
74A
82
66A
J1 DET
MF DET
WRITING CONTROL PART
80
76
COMPARING CONTROL PART
READING CONTROL PART
SEL CONT
SEL
RECEIVER PATH DATA (8BIT PARALLEL)
70B
66B
J1 DET
MF DET
WRITING CONTROL PART
72B
78
MEMORY
74B
60B
BIP OPERATING PART
ERROR DET
B3 DET
68B
RECEIVER PATH DATA FROM COMMUNICATION PATH β (8BIT PARALLEL)
PTR DET
62B
64B

FIG.13

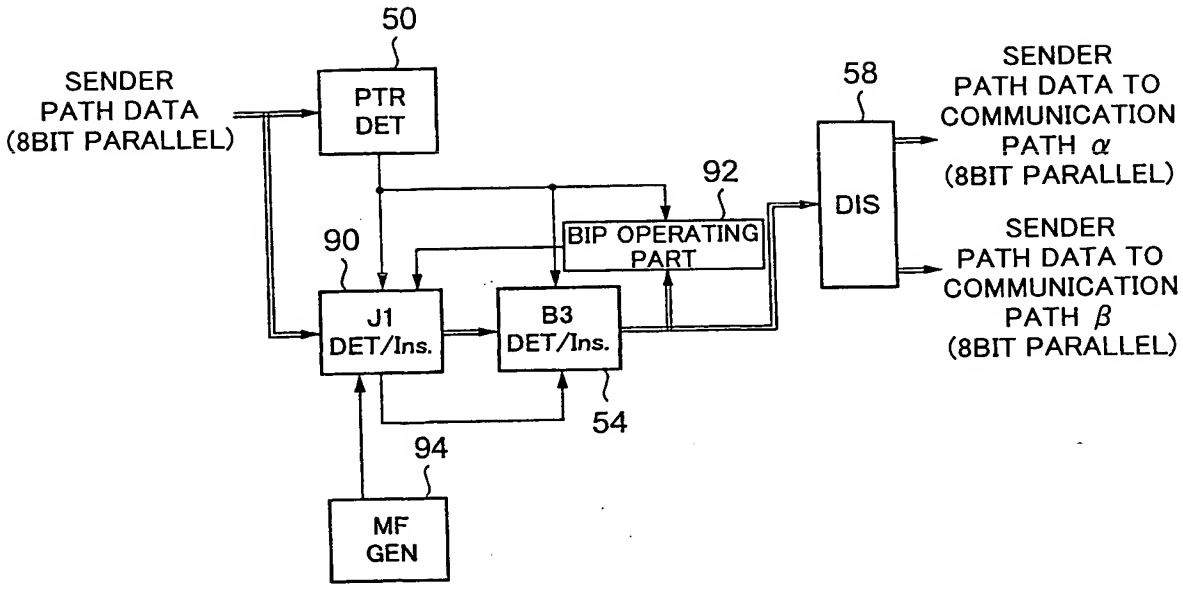

50
SENDER
PATH DATA
(8BIT PARALLEL)
PTR
DET
58
SENDER
PATH DATA TO
COMMUNICATION
PATH α
(8BIT PARALLEL)
92
DIS
BIP OPERATING
PART
90
SENDER
PATH DATA TO
COMMUNICATION
PATH β
(8BIT PARALLEL)
J1
DET/Ins.
B3
DET/Ins.
54
94
MF
GEN

FIG.14

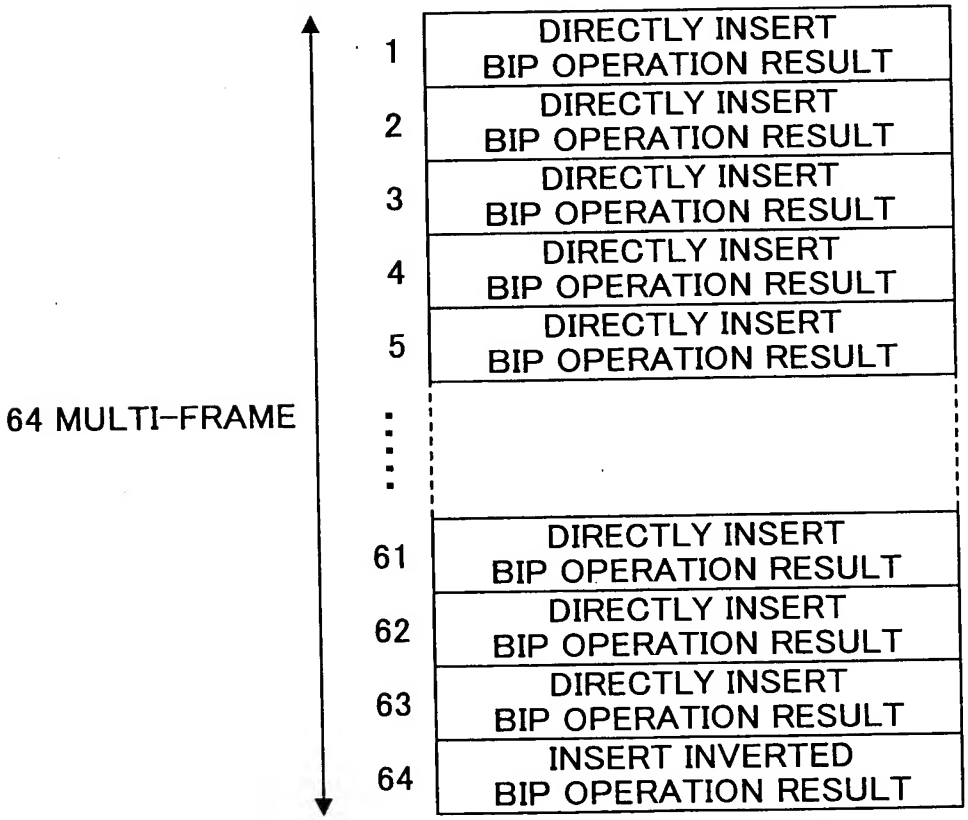
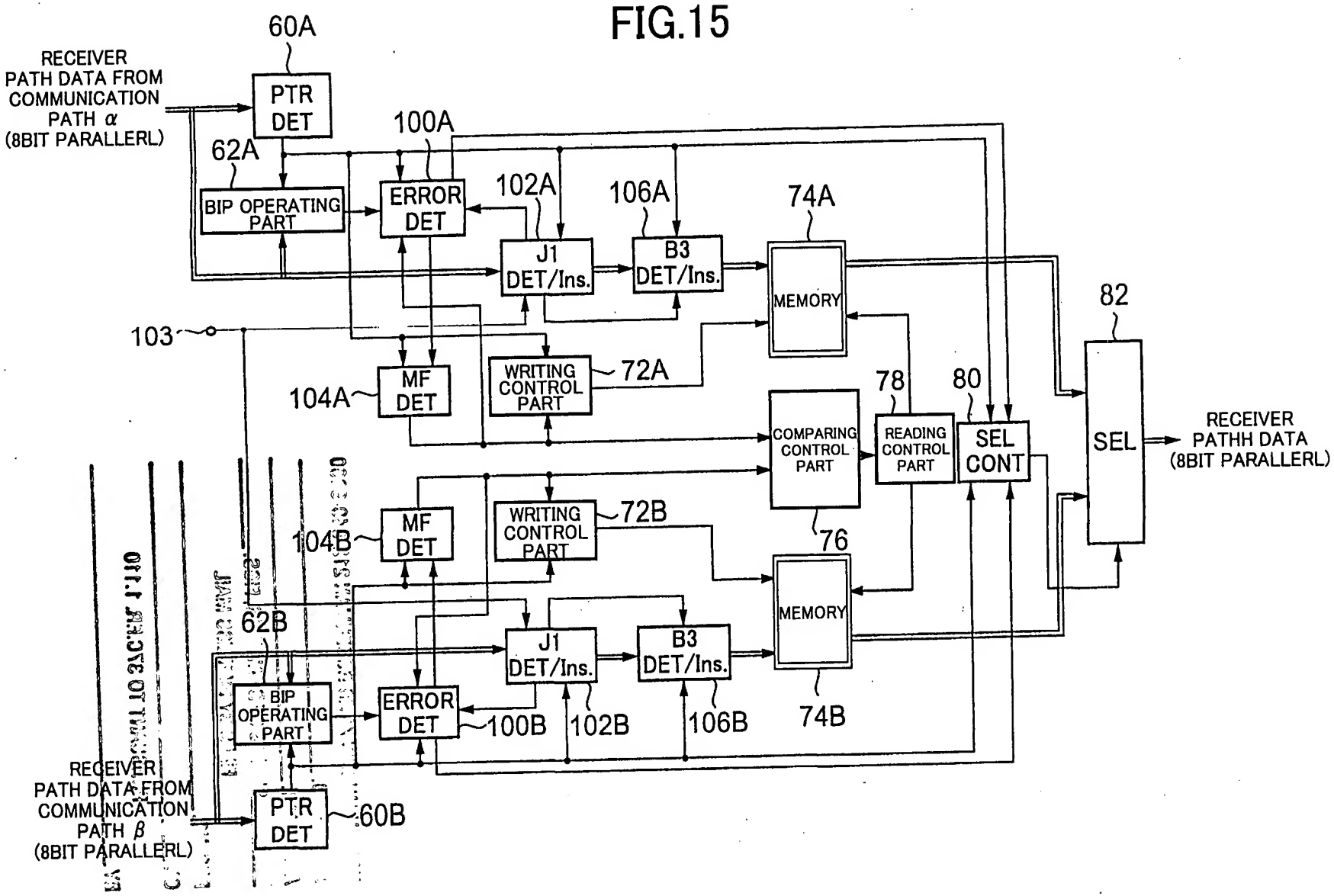

64 MULTI-FRAME
1
DIRECTLY INSERT
BIP OPERATION RESULT
2
DIRECTLY INSERT
BIP OPERATION RESULT
3
DIRECTLY INSERT
BIP OPERATION RESULT
4
DIRECTLY INSERT
BIP OPERATION RESULT
5
DIRECTLY INSERT
BIP OPERATION RESULT
61
DIRECTLY INSERT
BIP OPERATION RESULT
62
DIRECTLY INSERT
BIP OPERATION RESULT
63
DIRECTLY INSERT
BIP OPERATION RESULT
64
INSERT INVERTED
BIP OPERATION RESULT

FIG.15


RECEIVER PATH DATA FROM COMMUNICATION PATH α (8BIT PARALLERL)
60A
PTR DET
62A
BIP OPERATING PART
100A
ERROR DET
102A
J1 DET/Ins.
106A
B3 DET/Ins.
74A
MEMORY
82
103
MF DET
104A
WRITING CONTROL PART
72A
78
80
COMPARING CONTROL PART
READING CONTROL PART
SEL CONT
SEL
RECEIVER PATHH DATA (8BIT PARALLERL)
MF DET
104B
WRITING CONTROL PART
72B
76
MEMORY
62B
J1 DET/Ins.
B3 DET/Ins.
BIP OPERATING PART
ERROR DET
100B
102B
106B
74B
RECEIVER PATH DATA FROM COMMUNICATION PATH β (8BIT PARALLERL)
PTR DET
60B